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NOTICE OF ALLOWANCE AND FEE(S) DUE

21186

7590

04/20/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER

PAPER NUMBER

VESPERMAN, WILLIAM C

ART UNIT

DATE MAILED: 04/20/2004

APPLICATION NO.	FILING DATE FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/042 924	01/09/2002	Leonard Forbes	303 6841152	5327	

TITLE OF INVENTION: P-CHANNEL DYNAMIC FLASH MEMORY CELLS WITH ULTRATHIN TUNNEL OXIDES

APPLN, TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	07/20/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

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- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.
- Applicant claims SMALL ENTITY status.
 See 37 CFR 1.27.
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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO, on the date indicated below. SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402 (Depositor's name (Signature) (Date APPLICATION NO. FILING DATE FIRST NAMED INVENTOR ATTORNEY DOCKET NO. CONFIRMATION NO. 10/042.924 01/09/2002 303.684US2 5327 TITLE OF INVENTION: P-CHANNEL DYNAMIC FLASH MEMORY CELLS WITH ULTRATHIN TUNNEL OXIDES APPLN. TYPE SMALL ENTITY ISSUE FEE PUBLICATION FEE TOTAL FEE(S) DUE DATE DUE nonprovisional NO \$1330 \$300 \$1630 07/20/2004 **EXAMINER** ART UNIT CLASS-SUBCLASS VESPERMAN, WILLIAM C 2813 438-264000 1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). 2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required. attorneys or agents. If no name is listed, no name will be printed. 3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type) PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment. (A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY) Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ corporation or other private group entity ☐ government 🗖 individual 4a. The following fee(s) are enclosed: 4b. Payment of Fee(s): ☐ Issue Fee ☐ A check in the amount of the fee(s) is enclosed. ☐ Publication Fee □ Payment by credit card. Form PTO-2038 is attached. ☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number ______ (enclose an extra copy of this form). ☐ Advance Order - # of Copies Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. (Authorized Signature) (Date)

NOTE; The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

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P.O. BOX 2938 MINNEAPOLIS, MN 55402		402		ART UNIT	PAPER NUMBER	
	,			2813		
				DATE MAILED: 04/20/2004		

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 129 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 129 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

		AK			
	Application No.	Applicant(s)			
Notice of Allowability	10/042,924 FORBES, L		EONARD		
Notice of Allowability	Examiner	Art Unit			
	William C. Vesperman	2813			
The MAILING DATE of this communication appeal claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIOF the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this app or other appropriate communication IGHTS. This application is subject to	olication. If not include will be mailed in due	ed course. THIS		
1. X This communication is responsive to 4/15/04.					
2. \square The allowed claim(s) is/are <u>1-6 and 21-49</u> .					
3. \boxtimes The drawings filed on <u>08 March 2004</u> are accepted by the	Examiner.				
4. ☐ Acknowledgment is made of a claim for foreign priority un a) ☐ All b) ☐ Some* c) ☐ None of the: 1. ☐ Certified copies of the priority documents have 2. ☐ Certified copies of the priority documents have 3. ☐ Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)).	been received. been received in Application No		tion from the		
* Certified copies not received:					
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		complying with the rec	luirements		
 A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give 			OTICE OF		
 CORRECTED DRAWINGS (as "replacement sheets") must be submitted. (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached 1) ☐ hereto or 2) ☐ to Paper No./Mail Date (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 					
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t			back) of		
 DEPOSIT OF and/or INFORMATION about the depo- attached Examiner's comment regarding REQUIREMENT 			lote the		
 Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 9 / March 4,2004 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material 	5. Notice of Informal Page 1. Interview Summary Paper No./Mail Date 1. Examiner's Amendm 8. Examiner's Stateme 9. Other	(PTO-413), e nent/Comment	·		

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DETAILED ACTION

1. This action is in reply to applicant's amendment of 4/15/2004.

Allowable Subject Matter

- 2. Claims 1 6, 21 49 are allowed.
- 3. The following is an examiner's statement of reasons for allowance.

Hsu et al. (US 6,245,613) teaches (Figure 17) a method of forming a field effect transistor which includes: forming an oxide layer of 10 to 40 Angstroms on and contacting a substrate; forming a channel region separating the source and drain region in the substrate; forming a floating gate on and contacting the oxide layer; forming a dielectric layer on the floating gate; and forming a control gate on dielectric layer.

Hsu et al. does not teach forming an enhancement mode p-channel memory cell. In addition, Hsu et al. does not teach an oxide layer which contacts the substrate, the source, the drain and the channel regions; and wherein the p-channel memory cell is adapted to erase using a potential of magnitude of about 3 volts or less applied to the floating gate or that the enhancement mode p-channel memory cell has an operating voltage of less than 2.5 volts across the oxide layer.

Claims 1 - 6, 21 - 23

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming an oxide layer of less than 40 Angstroms on and

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contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and wherein the p-channel memory cell is adapted to erase using a potential of magnitude of about 3 volts or less applied to the floating gate or having an operating voltage of less than 2.5 volts across the oxide layer.

Claims 24 - 29

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming an oxide layer of less than 40 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and wherein the p-channel memory cell is adapted to have a reliability of a number of cycles of performance of approximately 10 to the twelve to 10 to the fifteen cycles over a life time of the enhancement mode p-channel memory cell; and having an operating voltage of less than 2.5 volts across the oxide layer.

Claims 30 - 32

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming an oxide layer of less than 30 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and wherein the p-channel memory cell is adapted to erase using a potential of magnitude of about 3 volts or less applied to the floating gate.

Claims 33 - 35

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The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming a plurality of memory cells, wherein at least one p-memory is formed and wherein one p-memory cell includes: forming an oxide layer of less than 23 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and having an operating voltage of approximately 1.0 volt applied to the control gate; and forming at least one sense amplifier that is coupled to the plurality of memory cells.

Claims 36 - 40

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode transistor which includes: forming an oxide layer of less than 40 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; forming a floating gate on and contacting the oxide layer, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10 to the seventeen Coulombs for longer than 1.0 hour at 20 degrees Celsius; forming a dielectric layer on the floating gate where the dielectric layer includes silicon dioxide; and forming a control gate on the dielectric layer.

Claims 41 - 46

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming a plurality of memory cells, wherein at least one p-

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memory is formed and wherein one p-memory cell includes: forming an oxide layer of less than 40 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; forming a floating gate on and contacting the oxide layer wherein the floating gate is adapted to hold a charge on the order of 10 to the seventeen Coulombs for longer than 1.0 hour at 20 degrees Celsius; and forming at least one sense amplifier that is coupled to the plurality of memory cells.

Claims 47 - 49

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel transistor which includes: forming an oxide layer of less than 23 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and forming a floating gate on and contacting the oxide layer wherein the floating gate is adapted to hold a charge on the order of 10 to the seventeen Coulombs for longer than 1.0 second at 85 degrees Celsius.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ying Shi, Xiewen Wang and T. P. Ma, <u>Tunneling Leakage Current in</u>

<u>Utrathin Nitride/Oxide Stack Dielectrics</u> (Published IEEE, 1998, pages 388 – 390)

teaches using a ultra-thin nitride/oxide stack comprising of a SiN layer and a

SiO2 layer formed over the SiN layer in order to replace a conventional oxide insulating layer.

Yang et al. (US 6,515,328) teaches a semiconductor devices with reduced control gate dimensions.

Yang et al. (US 6,383,939 B1) teaches a method of etching a memory gate stack.

Chang et al. (US 2003/0001197 A1) teaches a method for forming a memory cell having a contoured floating gate.

Chuang et al. (US 5,869,370) teaches forming a thin tunneling oxide layer using CVD.

Chung (US 2003/0201491 A1) teaches a semiconductor device containing oxide/nitride/oxide insulating stack layers.

Chang (US 5,408,115) teaches a self aligned EEPROM device.

Wu (US 6,316,316) teaches a method of forming high density flash memories.

Lin et al. (US 6246089) teaches flash EEPROM devices.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl White, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

wcv

Art Unit 2813

C. Chardhari

April 17, 2004

Chandra Chaudhari Primary Examiner